REMARKS

The Examiner has stated that claim 7 would be allowable. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter

The Examiner rejected claims 1-7 and 21-22 under 35 U.S.C. 112 (second paragraph).

The Examiner rejected claims 1-6 and 15-22 under 35 U.S.C. 102(e) as being anticipated by Murai et al. et al. (6,496,429).

Applicants respectfully traverse the §112 and §102(e) rejections with the following arguments.

35 USC § 112

The Examiner rejected claims 1-7 and 21-22 under 35 U.S.C. 112 (second paragraph).

As per claim 1, the Examiner stated "claim 1, 1ine 3, :said 'DDR DRAM' does not have clear antecedent basis." In response Applicants respectfully point out that in the amendment filed on May 19, 2006, Applicant amended step (a) of claim 1 to state "placing **a** DDR DRAM having a test mode and an operational mode in test mode." This same change was made to claim 15 in the response of May 19, 2006. Applicants believe there is currently no antecedent basis problem with claim 1.

As per claims 21 and 22, the Examiner stated " the step with letter 'f' already exists in claim 1"[and 15]. In response, Applicants have amended claims 21 and 22 replace a step 'f' with 'h'."

35 USC § 102 Rejections

Applicants respectfully point out that Murai et al. teaches simultaneously testing a bitline in a normal array and a bitline in a spare array at the same time while Applicants invention is performing a burn-in test of a DDR DRAM in a novel manner to eliminate exceeding the retention time specification of the DDR DRAM during testing. Therefore the invention of Murai et al. is fundamentally different from Applicants invention and since Murai et al. does not include the modifications to the DDR DRAM taught as required by the Applicant, Murai et al. cannot perform the operations taught and claimed by Applicants.

Further, the Examiner pointed to "(See col. 5, lines 1-20, col. 6, lines 34-42, col. 10, lines 16-30 and col. 24, lines 40-67 to col. 24, lines 1-10)." as the basis for the 35 USC §102(e) rejection. Applicants respectfully point out that col. 5, lines 1-20 and col. 6, lines 34-42 describe prior art and col. 24, lines 40-67 to col. 24, lines 1-10 describe the invention of Murai et al. and that such a combination does not satisfy the "identically disclosed" requirement of a 35 USC §102(e) reference.

More specifically:

As per claim 1 the Examiner states that "As per claims 1-6, Murai et al. et al disclose the invention substantially as claimed, comprising: a) placing a DDR DRAM having a test node and normal operational mode in test mode; b) issuing a bank activate command to select and bring up a wordline selected for write of the DDR DRAM; c) writing with auto-precharge is inherent in the system of Murai et al. et al, a test pattern to cells of the DDR DRAM; d) repeating steps (b) and (c) until all wordlines for write have been selected; (e) issuing a bank activate command to select and bring up a wordline selected for read of the DDR DRAM; (f) reading with auto-precharge is inherent in the system of Murai et al. et al, the stored test pattern from cells of DDR

DRAM; and (g) repeating steps (e) and (f) until all wordlines read have been selected. (See col. 5, lines 1-20, col. 6, lines 34-42, col. 10, lines 16-30 and col. 24, lines 40-67 to col. 24, lines 1-10). As per claims 15-22, these claims are rejected under similar rationale as set forth in claims 1-6."

Applicants contend that claim 1, as amended, is not anticipated by Murai et al. because Murai et al. does not teach each and every feature of claim 1

As a first example Murai et al. does not teach "(b) issuing a bank activate command on an occurrence of a rising edge of a first clock signal of a pair of adjacent clock signals of a test clock to select and bring up a wordline selected from said set of wordlines for write of said wordline selected for write."

As a second example Murai et al. does not teach "issuing a write with auto-precharge command on an occurrence of a rising edge of a second clock signal of said pair of adjacent clock signals to write a test pattern to storage cells corresponding to said wordline selected for write." as Applicants claim 1 requires.

As a third example Murai et al. does not teach "(e) issuing a bank activate command on a rising edge of a first clock signal of a subsequent pair of adjacent clock signals to select and bring up a wordline selected for read of said set of wordlines."

As a fourth example Murai et al. does not teach "issuing a read with auto-precharge command on an occurrence of a rising edge of a second clock signal of said subsequent pair of adjacent clock signals to read the stored test pattern from storage cells corresponding to said wordline selected for read."

Applicants point out that Murai et al. does not discuss clock signals in the context of commands during test mode. Rather Murai et al. discusses clock signals to the circuits attached

to the bitlines to control connections to the bitlines of the normal and spare arrays. The one time Murai et al. mentions rising and falling clock edges in a description of the normal operation and not test mode of a DDR DRAM in col. 24, lines 45-48.

The Examiner stated that "writing with auto-precharge is inherent in the system of Murai et al" and "reading with auto-precharge is inherent in the system of Murai et al." Applicants point out that inherent means existing as an essential constituent or characteristic. There are many methods of pre-charging bitlines possible and Murai et al. is silent as to the method used. For example, Applicants teach in Applicants FIG. 2, and paragraphs [0018-0021] a first method wherein the precharge (PRE) command is issued three clocks after the write command (WR) and the PRE command is issued two clock cycles after the read (RD) command and then teach in FIG.3 and paragraphs [0022-0029] issuing the write and precharge commands as a single write with auto-precharge (WR/AP) command and issuing the write and precharge commands as a combined read with auto-precharge (RD/AP) command. Further Murai et al. does not teach the modifications to the DDR DRAM necessary to accept WR/AP and RD/AP commands. Therefore auto-precharge in not inherent in Murai et al.

As a fifth example Murai et al. does not teach "repeating steps (b) and (c) until all wordlines of said set of wordlines have been selected and written" as Applicants claim 1 requires.

As a sixth example Murai et al. does not teach "(g) repeating steps (e) and (f) until all wordlines of said set of wordlines have been selected and read."

Applicants point out Murai et al. does not describe the details and sequence of writing and reading of test patterns to the cells of the normal and spare arrays so it is only supposition to assume and particular sequence for reading and writing. For example, it is possible to write one

wordline, read the bits in that wordline and then write another wordline and read the bits in that wordline and so on.

Based on the preceding arguments, Applicants respectfully maintain that claim 1 is not unpatentable over Murai et al. is in condition for allowance. Since claims 2-7 and 21 depend from claim 1, Applicants respectfully maintain that claims 2-7, 21, 23, 25, 27 and 29 are likewise in condition for allowance.

As per claim 2, Applicants find no teaching in Murai et al. that "a read column address select latency of said DDR DRAM is one clock cycle of said test clock.." Therefore, Applicants maintain claim 2 in condition for allowance.

As per claim 3, Applicants find no teaching in Murai et al. that "before step (a), the step of heating said DDR DRAM to an elevated temperature greater than room temperature." Applicants find no teaching of test temperature in Murai et al. Therefore, Applicants maintain claim 3 in condition for allowance.

As per claim 4, Applicants find no teaching in Murai et al. that "wherein said DDR DRAM is operating at a clock frequency below about one MHz in said test mode." In fact, Applicants can not find the words "frequency" or "MHz" in Murai et al. Therefore, Applicants maintain claim 4 in condition for allowance.

As per claim 5, Applicants find no teaching in Murai et al. that "wherein an amount of elapsed time between writing to and reading from a storage cell accessible by a particular

wordline and bitline combination does not exceed a retention time specification of said storage cell." In fact, Applicants can not find the words "retention time" or even "retention" in Murai et al. Therefore, Applicants maintain claim 5 in condition for allowance.

As per claim 6, Applicants find no teaching in Murai et al. that "wherein peripheral logic circuits of said DDR DRAM are adapted to execute a write burst enable and a column address command one clock cycle earlier in test mode than in operational mode, adapted to execute an auto-precharge enable one-half clock cycle earlier in test mode than in operational mode, and having a column address latency of one clock cycle in test mode and two or three clock cycles in operational mode." Applicants find no teaching in Murai et al. of differences in the timing of signals between test and normal mode. Therefore, Applicants maintain claim 5 in condition for allowance

Applicants contend that the arguments present *supra* with respect to claims 1-6 also apply to corresponding claims 15, 16, 19 and 20 and therefore claims 15, 16, 19, 20, 22, 24, 26, 28 and 30 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0458.

Respectfully submitted,
FOR: Norris et al.

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